

PBT8812 / PBT4412

112Gbps/ch Bit Error Ratio Tester

Version 1.9





Product Description

Semight Instruments PBT8812/PBT4412 is a high-performance bit error ratio tester (BERT) applied to high-speed serial signal error rate test, which can be used for physical layer characterization and consistency test. It covers emerging 200/400/800GbE and CEI-112G standards by virtue of support for 4-level pulse amplitude modulation (PAM4) signals with up to 56 Gbaud symbol rate (equivalent to 112 Gbps), as well as non-return-to-zero (NRZ) signals. It provides strong performance and flexibility guarantee for pre-research, design and production test of high-speed serial circuit product based on its excellent signal quality (fast rise/fall time, low jitter), rich functions (supporting real FEC analysis), flexible feature options and ultra-high overall integration. Moreover, the programmable pattern generator (PPG) can provide 3-Tap/7-Tap pre-emphasis tuner to compensate the loss of the signal in the transmission process and improve the signal quality. The bit error detector (ED) is equipped with built-in equalizer to ensure the signal integrity of the link. Moreover, the built-in fast locked clock recovery module ensures the stability of the link during the bit error test and the accuracy of the bit error test in the harsh and complex test environment.

Key Features

- High performance 112 Gbps/Ch bit error ratio tester, supporting up to 8 (PBT8812) or 4 (PBT4412) groups of service channels;
- Fast rising edge, low jitter;
- Support real pcs layer FEC analysis;
- Built-in RF switch to achieve host remote-switching trigger clock port;
- Each channel can be independently configured as NRZ or PAM4;
- Support symbol rate range: 24.33-56.25 Gbaud;
- Powerful receiving end feature with histogram and SNR measurement.
- 3-Tap and 7-Tap emphasis tuner with pre/main/post tap adjust;
- Support random/burst bit error injection and input/output polarity inverse;
- Clock out supports frequency division (1/4~1/128 ratio);
- Powerful and flexible database management function, giving assistance to research and development of in-depth analysis of data;
- The product can be flexibly programmed by calling external API (LabVIEW, C #) through Ethernet port or USB control interface;
- Support rich test patterns:
 - PRBS 7/9/11/13/15/16/23/31;
 - PRBS 7~31Q;
 - SSPRQ test pattern;
 - Square Wave, JP03A, JP03B, CJT, LIN;
 - User-defined test pattern (64 bits length);



Software Function

Semight Instruments PBT8812/PBT4412 has very intuitive and simple interface GUI in which the system features can be easily configured.

BER statistics can be displayed with SNR indicator together. BER/FEC real-time plots give assistance on capturing alarm events easily.

The real FEC analyzer provides PCS layer framing generator and gives user better evaluation on pre/post error symbols.

The screenshot shows the PPG configuration interface. At the top, it displays 'COM SELECT: COM17', 'LAN Port', 'Disconnect', 'Date Rate: 53.12500 GBaud', 'Trig: Rate/8', 'Trig A', and 'FEC OFF'. Below this are tabs for 'CH1-CH4', 'CH5-CH8', and 'Monitor'. A green bar contains 'LOG Manager', 'PAM4', 'PPG OFF ALL', 'BER STOP ALL', 'CLEAR ALL', and 'AUTOALIGN'. The main area is divided into four channel panels (CH1, CH2, CH3, CH4). Each panel includes:

- PPG Pattern: PRBS16Q
- ED Gating Times (s): 10000000
- PPG Amplitude (%): 90.0
- 900 mVpp
- Pattern Detected: PRBS16Q
- Polarity Detected: NORM
- Elapsed Time: 13s (for CH1, CH2, CH4) or 12s (for CH3)
- Error Count LSB, Error Ratio LSB, Error Count MSB, Error Ratio MSB
- Buttons: PPG OFF, STOP ED, CLEAR, PG, ED, LOCK, Err Inj, COMBINED, ON
- SNR indicator: 2.90dB (for CH1, CH2) or 3.30dB (for CH3) or 3.55dB (for CH4)

The screenshot shows the FEC analysis interface. At the top, it displays 'COM SELECT: COM17', 'LAN Port', 'Disconnect', 'Date Rate: 53.12500 GBaud', 'Trig: Rate/8', 'Trig A', and 'FEC ON'. Below this are radio buttons for '200G KP4' and '400G KP4', and a dropdown for 'All Channels'. A green bar contains 'STOP', 'CLEAR', and 'AUTOALIGN'. The left panel shows configuration parameters:

- Lock: ON
- Cor_Bits: 6107945
- Cor_CW: 5614786
- Cor_BitsRate: 1.06E-006
- Cor_CWRate: 5.30E-003
- UnCor_CW: 0
- UnCor_CWRate: 0.00E+000
- Total_CW: 1058374420
- Margin: 20%(max:12)
- Elapsd_Time: 6
- Gating_Time: 10000000

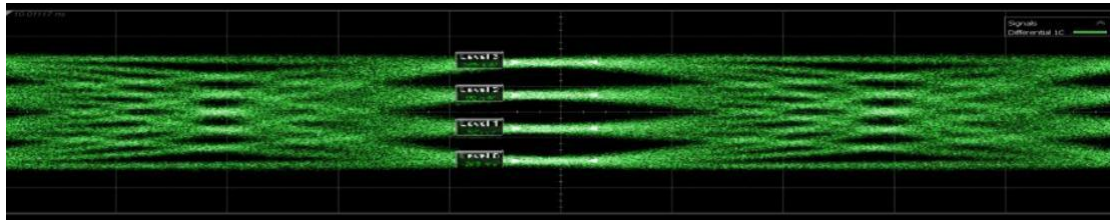
 The right panel features a 'FEC Plot' with 'CodeWord Count' on the y-axis (log scale from 1.0e+00 to 1.0e+07) and 'Symbol Error' on the x-axis (linear scale from 0 to 20). A legend indicates 'All' data points. Below the plot is a table:

Ch/Symbol	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	5379648	211384	19998	2933	610	146	40	17	5	3	1	1	0	0	0

 The bottom left panel includes 'LOG Manager' with 'Real-time Record' selected, 'Record Per: 6 Second', and 'Margin Alarm' with 'Threshold: 15' and 'OFF'.



Technical Specifications



*SSPRQ Pattern @ 53.125 Gbaud, differential eye diagram @ Keysight DCA 1092C

Pattern Generator Indicators	Output type	PAM4/NRZ
	Termination	Differential 100 Ω, Single-ended 50 Ω; AC-coupled
	Data patterns	PRBS 7/9/11/13/15/16/23/31, PRBS7~31Q
		SSPRQ, JP03A/03B, LIN, CJT, Square Wave
		User Defined Pattern (64bits length)
	Data symbol rate (Gbaud)	24.33/24.8832/25/25.78125/26.5625/27.89/27.95/28.05/28.125/28.2/28.9/30; ^① 48.66/49.7664/51.5625/53.125/56/56.25
	Frequency accuracy (Typical)	±50 ppm
	Maximum output amplitude (differential) ^②	650 mVp-p
	Rise time (20%–80%) ^③	<10 ps
	Fall time (20%–80%) ^③	<10 ps
Data output RMS jitter	<350 fs	
Connector	1.85 mm female, 50 Ω	

① Optional.

② Net measured value at Tx port.

③ Measured with 56.25Gbps NRZ signal.

Trigger Output Indicators	Output amplitude	>300 mVp-p
	Output type	AC-coupled, Single-ended
	Frequency division ratio (settable)	4/8/16/32/128
	Connector	2.92 mm female, 50Ω
	Trigger output	Remotely switching clock output port with built-in RF switch. (Trig A for Ch1~4 and Trig B for Ch5~8)
Error Detector Indicators	Input type	Differential PAM4/NRZ
	Termination	AC-coupled
	Input impedance	100 Ω
	Receiving amplitude (differential) ^①	100 ~ 650 mVp-p
	Receiving sensitivity (differential) ^②	100 mVp-p
	Data patterns	PRBS 7/9/11/13/15/16/23/31, PRBS7~31Q



	Data symbol rate (Gbaud)	24.33/24.8832/25/25.78125/26.5625/27.89/27.95/28.05/28.125/28.2/28.9/30; ^③ 48.66/49.7664/51.5625/53.125/56/56.25
	SNR indicator	Support
	Clock mode	Built-in clock recovery
	Synchronization type	Auto Synchronization (level/phase)
	Connector	1.85 mm female, 50 Ω

① Net measured at Rx port.

② BER might reach to E-3 level or even LOS while input signal <100mVp-p.

③ Optional.

General Indicators	Environment	Indoor
	Work	0°C~+55°C, 30%~80% Relative Humidity with no condensation
	Storage	-30°C~70°C, 10%~90%Relative Humidity with no condensation
	Altitude	Operation: 0m to 2000m, Storage: 0m to 4600m
	Power	LINE:100~240 VAC,50/60 Hz,50 W
	Warm-up time	10 minutes
	Dimensions (mm)	412*441*112 (with foot pad/handle)
	Weight	Net weight 7.0 kg

Ordering Information

Product Model	Product Description
PBT8812	8×112 Gbps Bit Error Ratio Tester
PBT4412	4 x112 Gbps Bit Error Ratio Tester
Standard Accessories	Power cord, USB cable, Measurement Software and Drivers
Options	
-RFSW	Built-in RF switch which allows host remote-switching trigger clock port
-FEC	Built-in integrated real FEC analyzer, providing graphical analysis interface and data management
-EDR	Extendable Data Rate for more applications



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*This information is subject to change without notice.